Some Considerations for Optimal Efficiency and Low Noise in Large Power Combiners

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***Abstract*—This paper examines some relationships between important design parameters in large combiner systems and key performance objectives such as power, efficiency, noise, and graceful degradation. Results are derived for the combining efficiency of general combiner systems, and used to contrast spatial and corporate combiners and identify optimum combiner topology for a given device technology. The influence of array size on excess phase noise is quantified and shown to decrease with increase numbers of devices. Results are also presented for the degradation in combining efficiency due to statistical variations in amplifier characteristics, appropriate to large combiners, showing that phase errors are the dominant factor in power degradation.**

***Index Terms*—Combining efficiency, power amplifiers, power combining, spatial power combining.**

I. Introduction

HIGH power levels can be achieved in microwave/RF systems by combining the outputs of a number of amplifiers with otherwise limited power-handling capacity. The individual amplifiers are assumed to have roughly identical characteristics, and the splitter/combiner circuits are designed for uniform phase and amplitude characteristics over all N ports in the frequency band of interest, where N is the number of amplifiers to be combined. The passive combiner structure should have the lowest possible loss for efficient collection of available power.

To achieve a target power level, a designer will typically select the largest available power device (largest possible active die area) to minimize N and, hence, the complexity of the splitter/combiner networks. However, this design practice should be reconsidered if high efficiency and low phase-noise degradation are important objectives. It may be more advantageous to use a large number of smaller area devices to achieve a given power level since the smaller devices often have significantly higher power-added-efficiency (PAE) than large area devices (Fig. 1). There are other secondary benefits. Smaller devices yield better in production and, hence, can have lower overall cost. The excess phase noise through a combiner system is reduced by $1/N$ compared with the noise contributed by a single one of the component amplifiers—in other words, the degradation in phase noise through the amplifier can be reduced using a large number of amplifiers. Graceful degradation characteristics and tolerance of statistical device gain variations can also be improved using large numbers of devices.

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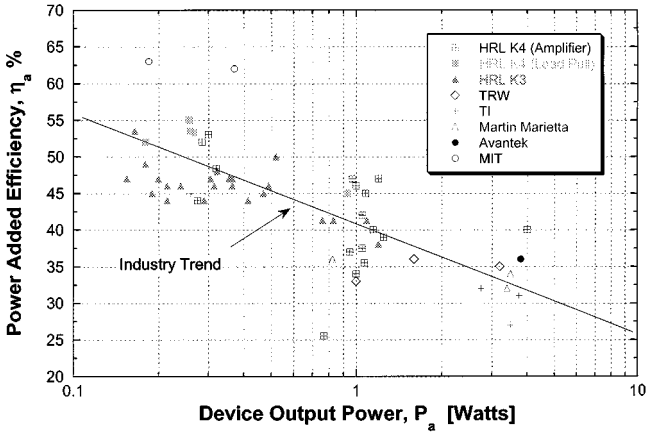

Fig. 1. Industry comparison of 18-GHz power devices [1].

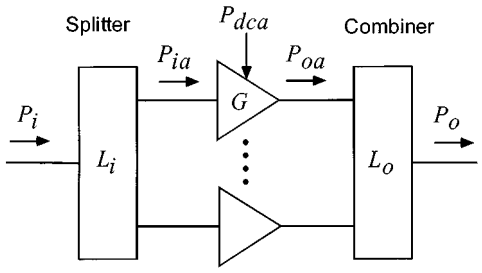

Fig. 2. General N-way power combiner system.

Small-area devices also facilitate wide-band circuit design, which may be advantageous in some applications.

To exploit these advantages requires an ability to combine large numbers of devices efficiently. Recent advances in spatial combining techniques offer an attractive means of doing so [2]–[5]. This paper examines some relationships between important design parameters in large combiner systems and performance objectives of combining efficiency, noise, and tolerance to device variations and failures.

II. Combining Efficiency and PAE

A general combiner system can be represented, as shown in Fig. 2, with a lossy input distribution network or "splitter," feeding a set of N amplifiers, and a lossy output combiner network.

The power transmission factor through the input and output splitter/combiner networks are described by L_i and L_o, respectively (e.g., a 3-dB loss in the output network corresponds to $L_o = 0.5$). Output losses determine the combining efficiency.

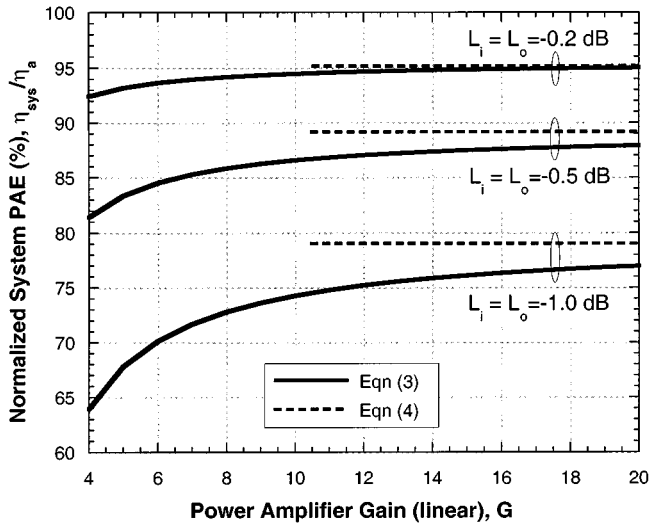

Fig. 3. Normalized PAE of a combiner system versus amplifier gain from (3).

Assuming a well-matched and balanced combiner with identical devices, the combining efficiency is

$$\eta_c = \frac{P_o}{NP_{oa}} = L_o. \tag{1}$$

Now consider the overall PAE. Each individual amplifier in Fig. 2 has a PAE defined as

$$\eta_a = \frac{P_{oa} - P_{ia}}{P_{\mathrm{dc}a}} = \frac{P_{ia}(G-1)}{P_{\mathrm{dc}a}}. \tag{2}$$

For the purpose of this analysis, we consider this number to be fixed by the choice of device technology or specification of the device size (Fig. 1). The purpose of the combiner system is then to combine a large number of such amplifiers with the least possible degradation in PAE relative to η_a. Using the notation of Fig. 2 and (2), we find an overall PAE for the general combiner system given by

$$\eta_{\mathrm{sys}} = \frac{P_o - P_i}{P_{\mathrm{dc}}} = \frac{P_i(L_iGL_o - 1)}{NP_{\mathrm{dc}a}} = \frac{(L_iGL_o - 1)}{L_i(G-1)}\,\eta_a. \tag{3}$$

From this result, we can see that, as the individual amplifier gain G increases, the loss in the input network becomes less significant.

Fig. 3 displays the overall PAE normalized to that of a single amplifier ($\eta_{\mathrm{sys}}/\eta_a$) as a function of amplifier gain for representative values of splitter and combiner loss. In the limit of high gain, we find

$$\eta_{\mathrm{sys}} \to \eta_a\eta_c. \tag{4}$$

For high gain, the normalized system PAE asymptotically approaches the combining efficiency. High gain in the system can compensate for the effect of input losses on efficiency, and should, therefore, be an important design objective for efficient combiners. Note, however, that Fig. 3 implicitly assumes the gain can be increased without increasing the dc power consumption of the array. Preamplifier stages, included either in each branch of the combiner or at the input of the splitter network, will increase the power consumption. However, since the preamplifier operates on a lower power signal, it should be possible to achieve the desired gain with a relatively small increase in power consumption relative to the power-amplifier stage.

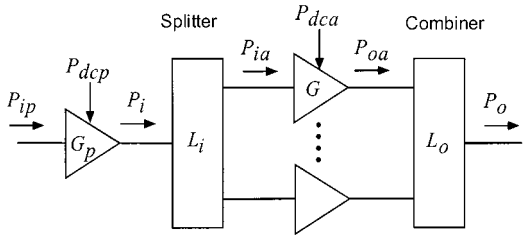

Fig. 4. General combiner system with preamplifier.

Consider the same power-combiner system of Fig. 1 with a preamplifier at the input, as shown in Fig. 4. Using the notation in Fig. 4, the overall system PAE can be expressed as

$$\eta_{\mathrm{sys}} = \frac{G_pL_iGL_o - 1}{\dfrac{1}{\eta_a}G_pL_i(G-1) + \dfrac{1}{\eta_p}(G_p - 1)} \tag{5}$$

where η_p is the PAE of the preamplifier defined as

$$\eta_p = \frac{P_{ip}(G_p - 1)}{P_{\mathrm{dc}p}}.$$

Note that when $L_i = L_o, \eta_p = \eta_a$, and $G = G_p$, this expression reduces to

$$\eta_{\mathrm{sys}} = \frac{GL_o - 1}{G-1}\,\eta_a \tag{6}$$

which is the same as (3) in the limit of no input loss. Hence, the system PAE should more rapidly approach the limiting value defined in (4) with the use of a preamplifier, even when the additional power consumption is accounted for.

Clearly, the output loss is a valuable figure-of-merit for characterizing a power-combining system. From an experimental point-of-view, it is usually easiest to measure the insertion loss through the entire passive network, which will include input and output losses. If the structure is symmetrical, a good estimate of the output losses can be obtained by halving the insertion loss. Estimates of output combining losses from measured data are provided in [2] and [4] for a spatial power combiner using this technique.

III. Influence of Combiner Topology

Spatial combiners are frequently argued to have potentially higher combining efficiency than transmission-line-based combiner systems. In fact, spatial combiners usually have poorer combining efficiency than transmission-line combiners when small numbers of elements are combined, owing to higher intrinsic losses in the passive structure, typically due to diffraction or higher order mode excitation.

The real advantage of spatial combiner (and other parallel schemes such as radial combiner) systems is that the combining

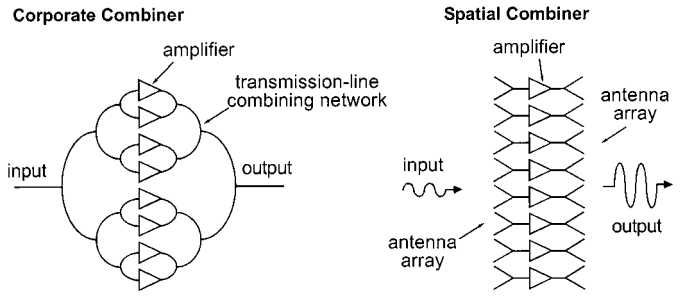

Fig. 5. Ideal binary-corporate and spatial combiners.

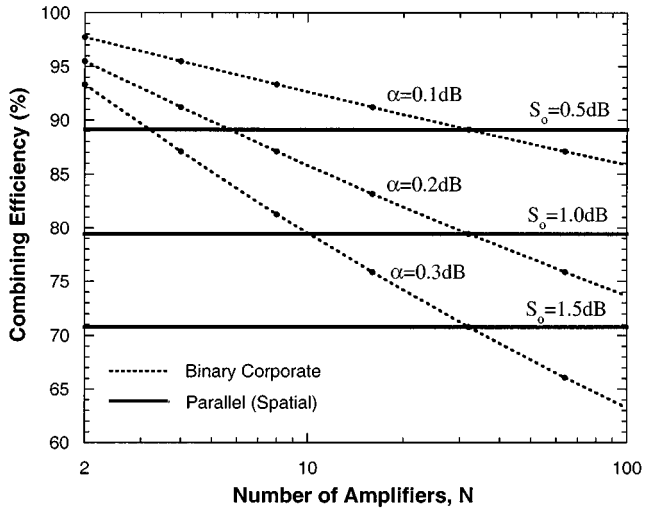

Fig. 6. Combining efficiency versus number of amplifiers.

efficiency is approximately independent of the number of devices. Experimental evidence for the constant combining efficiency versus number of devices is presented in [4] for combiner systems with up to 32 channels. In contrast, some transmission-line combiner systems (such as the corporate binary-combiner structure, as shown in Fig. 5) suffer a decrease in efficiency with increasing numbers of devices. This implies a critical number of devices beyond which parallel combining is more efficient.

An ideal binary-tree corporate combiner has a total output loss given by $L_o = \alpha^k$, where α is the loss per stage and $k = \log_2 N$ is the number of stages. An ideal spatial combiner has a constant output loss $L_o = S_o$. Fig. 6 compares the maximum combining efficiency for these two cases. The critical number of devices at which the corporate and spatial efficiency curves intersect is easily found as

$$N_c = 2^{S_o[\mathrm{dB}]/\alpha[\mathrm{dB}]} \tag{7}$$

where the loss terms are in decibels. For example, at X-band, $\alpha = 0.15$ dB is typical of a Wilkinson combiner, and $S_0 = 0.5$ dB for a spatial combiner, such as that described in [2] and [3]. Using these numbers, spatial combiners would be favored over a corporate structure at $N \geq 10$ for a given device. Note from Fig. 6 and (7) that the intersection point is sensitive to small differences in the binary-stage loss α.

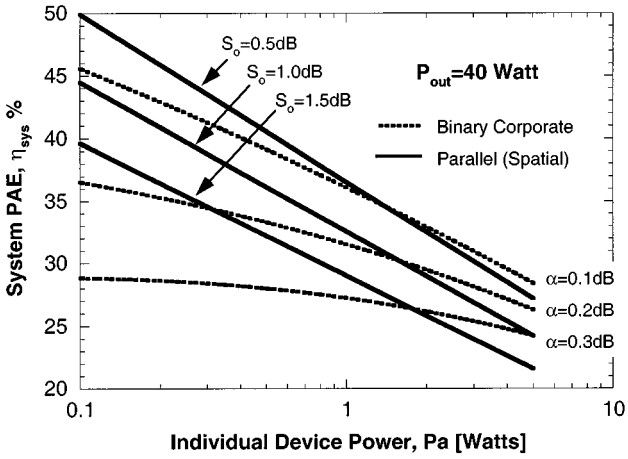

Fig. 7. Overall system efficiency as a function of device size, using the data of Fig. 1 and assuming a total output power of 40 W.

Fig. 6 and (7) are useful guides if the design objective is simply to maximize output power with the smallest number of devices. If design objectives include maximizing overall PAE, the influence of topology is especially interesting when the trends of Fig. 1 are accounted for. In this case, the problem to be addressed is as follows: given a range of available devices sizes $P_a^{\min} \leq P_a \leq P_a^{\max}$, a specified total output power P_{out}, and available combiner technologies specified by α and S_o, what is the best choice of device size and combiner topology to maximize overall system PAE?

In view of Figs. 1 and 6, note that if the specified output power is so large that $P_{\mathrm{out}} > N_c P_a^{\max} S_o$, then the spatial or parallel combiner topology will always be preferred, regardless of the choice of device. Expressed differently, this sets an upper bound on the device size that a spatial combiner must use to exceed the efficiency of a corporate combiner generating the same total power

$$P_a \leq \frac{P_{\mathrm{out}}}{N_c S_o}. \tag{8}$$

If $P_{\mathrm{out}} < N_c P_a^{\max} S_o$, the trend of Fig. 1 admits the possibility that a spatial combiner topology could still generate a higher efficiency than a corporate combiner, by using a larger number of smaller devices than the corporate combiner. For simplicity, we model the empirical trends in Fig. 1 using a linear approximation

$$\eta_a \approx A - B \log P_a. \tag{9}$$

The straight line in Fig. 1 corresponds to $A \approx 41\%$ and $B \approx 15\%$. Using (9), we can compute a system efficiency from (4) for a specified power level as a function of device size. This is done in Fig. 7, assuming a desired output power of 40 W at 18 GHz, with devices ranging in size from $P_a^{\min} = 0.1$ W to $P_a^{\max} = 5$ W (Fig. 1).

Fig. 7 is interesting in at least two respects. First, it demonstrates that the design practice of combining a minimum number of the largest available devices should be reconsidered, regardless of the choice of combiner topology, if maximum efficiency is an important objective. Second, under certain conditions, a parallel combiner structure can exceed the performance of even

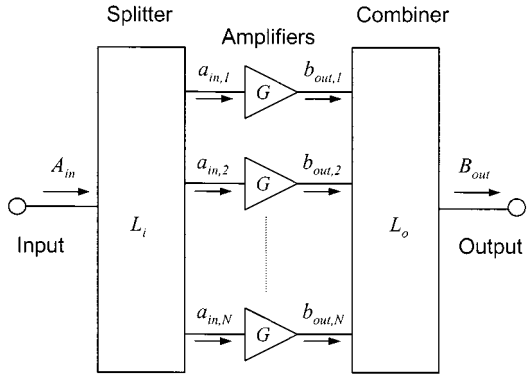

Fig. 8. Generic combiner system for noise analysis.

the most efficient corporate combiner if a large enough number of small devices are used. This regime is described by (8).

From another viewpoint, the implications of Figs. 1 and 7 is that on-chip combining (scaling the device area) is not very efficient relative to off-chip combining. The empirical data indicates approximately 2 dB of loss in efficiency with a factor of 16 increase in device power or area, or a 0.5-dB loss for every doubling of device power (approximately equivalent to doubling the device area). This is roughly equivalent to a corporate combiner with nearly 0.5 dB of loss per stage.

Naturally, economic issues and size constraints, neglected here, will be an important factor in determining the optimal number of devices. However, since small-area devices are generally less expensive (per unit area) than large-area devices, it seems reasonable to expect that large combiners with small area devices can be cost effective. The principal tradeoff is increased size and parts count.

IV. Phase Noise in Combiner Systems

The use of large numbers of small devices in a combiner can have a positive influence on the noise properties of the system. In transmitter applications, particularly for certain types of radar, the amplifier should not seriously degrade the phase noise of the signal to be amplified, which is typically generated from a source that is phase locked to a highly stable reference oscillator. The phase-noise reduction can be derived as follows, which roughly parallels earlier research aimed at noise reduction in oscillator systems [6].

With reference to the notation in Fig. 8, we assume the input signal to be amplified is a noisy signal of the form

$$A_{\rm in} = A\cos\left(\omega t + \delta\theta_{\rm in}\right) \tag{10}$$

where $\delta\theta_{\rm in}(t)$ describes the time-dependent phase fluctuations of the input signal. Assuming an ideal symmetric broad-band linear power splitter for simplicity, the input signal to each amplifier in the array can be represented as

$$a_{{\rm in},\,i} = \frac{A}{\sqrt{N}}\cos\left(\omega t + \delta\theta_{\rm in}\right). \tag{11}$$

The phase noise at the output of each amplifier is degraded, primarily from upconverted $1/f$ noise, due to the nonlinear devices in the amplifiers. Amplitude noise in the bias supplies can also be upconverted to near-carrier phase noise. For our purpose, the origin of the noise is unimportant, and we simply describe the total excess noise contribution of each amplifier by a time-domain fluctuation so that

$$b_{{\rm out},\,i} = \frac{AG}{\sqrt{N}}\cos\left(\omega t + \delta\theta_{\rm in} + \delta\varphi_i\right) \tag{12}$$

(note, G is now a voltage gain). The total output signal is then given by

$$\begin{aligned} B_{\rm out} &= \sum_{i=1}^{N}\frac{b_{{\rm out},\,{\rm i}}}{\sqrt{N}} = \frac{AG}{N}\sum_{i=1}^{N}\cos\left(\omega t + \delta\theta_{\rm in} + \delta\varphi_i\right) \\ &= AG\cos\left(\omega t + \delta\theta_{\rm out}\right). \end{aligned} \tag{13}$$

where

$$\delta\theta_{\rm out} = \delta\theta_{\rm in} + \frac{1}{N}\sum_{i=1}^{N}\delta\varphi_i.$$

In deriving this, we have assumed the phase fluctuations are small. We now assume that the input and amplifier noise sources are uncorrelated random (ergodic) processes with zero time average, and apply the Wiener–Khintchine theorem [7] to compute the power spectrum of the noise fluctuations. If the amplifiers have roughly the same noise power spectral density, the power spectral density of the output signal phase fluctuations (i.e., the phase noise of the output signal) will be given by

$$\left|\delta\tilde{\theta}_{\rm out}\right|^2 = \left|\delta\tilde{\theta}_{\rm in}\right|^2 + \frac{1}{N}\left|\delta\tilde{\varphi}\right|^2 \tag{14}$$

where $|\delta\tilde{\theta}_{\rm in}|^2$ represents the noise spectrum associated with the input signal, $|\delta\tilde{\varphi}|^2$ represents the excess phase noise contributed by a single amplifier, and the tilde (~) denotes a Fourier transform (defined in the usual way for a random process). This result shows that the phase noise contributed by the amplifier ensemble is reduced by $1/N$, as predicted. Intuitively, this is not surprising since the input signal being amplified adds coherently at the output, whereas the uncorrelated noise fluctuations add incoherently and, hence, the peak amplitude of the carrier increases more rapidly than the noise skirts.

V. Influence of Statistical Variations and Device Failures on Power and Efficiency

The influence of device failures on the power degradation characteristics of combiners has been addressed in [8], in which it was shown that, in a well-matched system, the reduction in power is expected to be proportional to $(1 - m/N)^2$, where m/N is the fraction of failed devices. However, in most cases, the system can actually perform better than this, depending on the impedance of the failed devices and the s-parameters of the combiner structure. This observation forms the basis of design schemes to improve graceful degradation performance (e.g., [9]). Recent measurements on laboratory combiner systems are shown in Fig. 9 and confirm this point. Such graceful

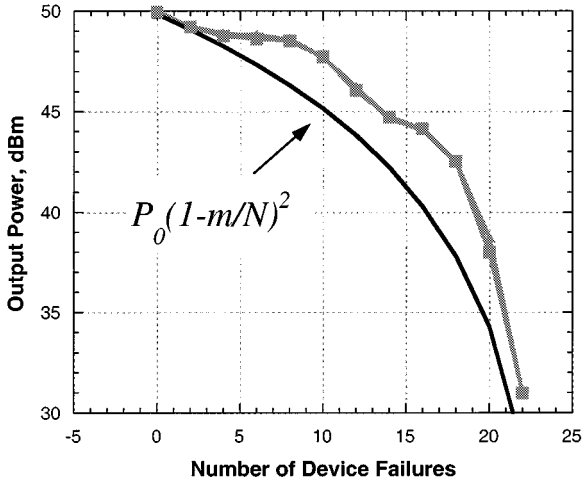

Fig. 9. Measured data (previously unpublished) for the combiner system reported in [3], with device failures simulated by removal of bias (▲ and □ denote two different shutdown sequences). The archetypal failure model [8] is shown for comparison ($N = 24$).

degradation characteristics are highly desirable in modern amplifier systems.

The efficiency of any real combiner is also limited by channel-to-channel uniformity. Gain and phase variations arising from device nonuniformities or manufacturing tolerances can lead to imperfect summation of power and, hence, a reduction in combining efficiency. This problem has been nicely treated in [10], in which the worst-case combining efficiency is quantified for a specified maximum phase and gain variation. Knowledge of the worst-case efficiency can be useful for conventional combiners. For large combiners with essentially random gain and phase variations, the probable efficiency is of interest, and a statistical treatment of the problem is appropriate. The problem is similar to the study of random errors in phased arrays, and the following closely parallels [11]. Using the notation of Fig. 8, we can write the output signal in phasor form as

$$B_{\text{out}} = \frac{AG_0}{N} \sum_{i=1}^{N} r_i(1+\delta G_i)e^{j\,\delta\varphi_i} \tag{15}$$

where

G_0 nominal amplifier voltage gain;
δG_i ith-channel amplitude error;
$\delta\varphi_i$ ith-channel phase error;
r_i statistical device failures.

The amplitude and phase errors are again assumed to be independent random processes with zero mean. The probability of device survival is represented by P_e such that $r_i = 1$ with probability P_e or $\langle r_i\rangle = P_e$. The output power is proportional to $P = B_{\text{out}}^2$. If we denote the "no-error" output power as $P_0 = (AG_0)^2$, then the relative change in the presence of errors is

$$\frac{P}{P_0} = \frac{1}{N^2} \sum_{i=1}^{N}\sum_{j=1}^{N} r_i r_j(1+\delta G_i)(1+\delta G_j)e^{j(\delta\varphi_i-\delta\varphi_j)}. \tag{16}$$

Separating out the terms with $i = j$ gives

$$\frac{P}{P_0} = \frac{1}{N^2}\left[\sum_{i=1}^{N} r_i^2(1+\delta G_i)^2 + \sum_{i=1}^{N}\sum_{\substack{j=1\\ j\neq i}}^{N} r_i r_j \cdot (1+\delta G_i)(1+\delta G_j)e^{j(\delta\varphi_i-\delta\varphi_j)}\right]. \tag{17}$$

Now taking the ensemble average and assuming the individual amplitude and phase errors have the same variance (rms value) gives

$$\frac{\langle P\rangle}{P_0} = \frac{P_e}{N}\left(1+\langle\delta G^2\rangle\right) + \frac{P_e^2}{N^2}\sum_{i=1}^{N}\sum_{\substack{j=1\\ j\neq i}}^{N}\left\langle e^{j(\delta\varphi_i-\delta\varphi_j)}\right\rangle \tag{18}$$

where we used $\langle r_i^2\rangle = \langle r_i\rangle$ since $r_i = 0$ or 1. Assuming the phase errors have a normal (Gaussian) distribution, Skolnik [11] has shown that

$$\left\langle e^{j(\delta\varphi_i-\delta\varphi_j)}\right\rangle = e^{-\langle\delta\varphi^2\rangle}$$

thus, we find

$$\frac{\langle P\rangle}{P_0} = P_e^2 e^{-\langle\delta\varphi^2\rangle} + \frac{1}{N}\left[P_e\left(1+\langle\delta G^2\rangle\right) - P_e^2 e^{-\langle\delta\varphi^2\rangle}\right]. \tag{19}$$

This is the desired result. The second term on the right-hand side becomes small for large N, thus, we see that the dominant effect is a power degradation due to device failures and phase errors. Large combiner systems can evidently tolerate significant amplitude errors as long as they have zero mean, but phase errors are particularly significant. For example, with an rms phase error of 45°, the power in a large array would be reduced by nearly 3 dB, seriously compromising combining efficiency and overall PAE. For small phase errors and $P_e = 1$, we find

$$\frac{\langle P\rangle}{P_0} \approx 1 - \langle\delta\varphi^2\rangle. \tag{20}$$

Extra care should be taken to minimize phase errors between channels. This is especially difficult at millimeter-wave frequencies, and has led some workers to include variable phase shifters in the combiner designs to compensate for device variations [12].

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